Bulk-synchronous pseudo-streaming for many-core accelerators

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Epiphany BSP

Extending BSP with streams

Examples

Inner product

Matrix multiplication

Sort



- 'A supercomputer for everyone, with the lofty goal of democratizing access to parallel computing'
- Crowd-funded development board, raised almost \$1M in 2012.



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- Efficient communication network with '*zero-cost start up*' communication. Asynchronous connection to *external memory pool* using DMA engines (used for software caching).
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- Each Epiphany core has 32 kB of **local memory**, on 16-core model 512 kB available in total. There are no caches.
- On each core, the kernel binary and stack already take up a large section of this memory.
- On the Parallella, there is 32 MB of **external RAM** shared between the cores, and 1 GB of additional RAM accessible from the ARM host processor.

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Epiphany BSP

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Hello World: ESDK (124 LOC)

// host

```
const unsigned ShmSize = 128;
const char ShmName[] = "hello_shm";
const unsigned SeqLen = 20;
```

```
int main(int argc, char *argv[])
```

```
unsigned row, col, coreid, i;
e_platform_t platform;
e_epiphany_t dev;
e_mem_t mbuf;
int rc:
```

```
srand(1);
```

```
e_set_loader_verbosity(H_D0);
e_set_host_verbosity(H_D0);
```

```
e_init(NULL);
e_reset_system();
e_get_platform_info(&platform);
```

```
rc = e_shm_alloc(&mbuf, ShmName,
        ShmSize);
if (rc != E_OK)
        rc = e_shm_attach(&mbuf, ShmName
        );
// ...
```

// kernel

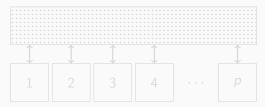
```
int main(void) {
    const char
                           ShmName[] = "
         hello_shm":
    const char
                       Msg[] = "Hello_
         World_from_core_0x%03x!";
    char
                       buf[256] = \{0\};
    e coreid t
                           coreid :
    e_memseg_t
                           emem :
    unsigned
                       my_row;
    unsigned
                       mv_col:
```

```
// Who am 1? Query the CoreID from
    hardware.
coreid = e_get_coreid();
e_coords_from_coreid(coreid, &my_row
    , &my_col);
if ( E_OK != e_shm_attach(&emem,
    ShmName) ) {
    return EXIT_FAILURE;
}
snprintf(buf, sizeof(buf), Msg,
    coreid);
```

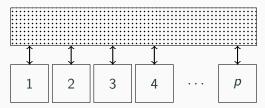
```
// ...
```

```
// kernel
// host
                                               #include <e_bsp.h>
#include <host_bsp.h>
#include <stdio.h>
                                               int main() {
                                                   bsp_begin();
int main(int argc, char** argv) {
    bsp_init("e_hello.elf", argc, argv);
                                                   int n = bsp_nprocs();
                                                   int p = bsp_pid();
    bsp_begin(bsp_nprocs());
                                                   ebsp_printf("Hello_world_from_core_%
    ebsp_spmd():
                                                         d/%d", p, n);
    bsp_end();
                                                   bsp_end();
    return 0:
                                                   return 0:
}
                                               }
```

- The BSP model [Valiant, 1990] describes a general way to perform parallel computations.
- An abstract BSP computer is associated to the model that has *p* processors, which all have access to a communication network.



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- BSP programs consist of a number of supersteps, that each have a computation phase, and a communication phase. Each superstep is followed by a barrier synchronisation.
- Each processor on a BSP computer has a processing rate *r*. It has two parameters: *g*, related to the communication speed, and *l* the latency.
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- Primary goal should be to minimize communication with external memory.
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- We view the Epiphany processor as a BSP computer with **limited local memory** of capacity *L*.
- We have a **shared external memory** unit of capacity *E*, from which we can read data **asynchronously** with **inverse bandwidth** *e*.
- Parameter pack: (p, r, g, l, e, L, E).

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- $r = (600 \times 10^6)/5 = 120 \times 10^6 \text{ FLOPS}^{(*)}$
- *l* = 1.00 FLOP
- g = 5.59 FLOP/word
- e = 43.4 FLOP/word
- L = 32 kB
- *E* = 32 MB

(*): In practice one FLOP every 5 clockcycles, in theory up to 2 FLOPs per clockcycle.

Extending BSP with streams

- *Idea:* present the input of the algorithm as **streams** for each core. Each stream consists of a number of **tokens**.
- The *i*th stream for the *s*th processor:

$$\Sigma_i^s = (\sigma_1, \sigma_2, \ldots, \sigma_n)$$

- Tokens fit in local memory: $|\sigma_i| < L$.
- We call the BSP programs that run on the tokens loaded on the cores hypersteps.

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Structure of a program

- In a hyperstep, while the computation is underway, the next tokens are loaded in (asynchronously).
- The time a hyperstep takes is either **bound by bandwidth or computation**.
- Cost function:

$$\tilde{T} = \sum_{h=0}^{H-1} \max\left(T_h, e\sum_i C_i\right).$$

Here, C_i is the token size of the *i*th stream, and T_h is the (BSP) cost of the *h*th hyperstep.

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- Here, by default the next logical token is loaded in. But programmer can *seek* within the stream.
- This minimizes the amount of code necessary for communication with external memory.
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```
// host
void* bsp_stream_create(
    int processor_id,
    int stream_size,
    int token_size,
    const void* initial_data);
```

// kernel
int bsp_stream_open(int stream_id);
void bsp_stream_close(int stream_id);

int bsp_stream_move_up(
 int stream_id,
 const void* data,
 int data_size,
 int wait_for_completion);

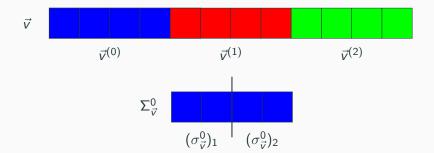
void bsp_stream_seek(
 int stream_id,
 int delta_tokens);

Examples

Example 1: Inner product

• Input: vectors \vec{v}, \vec{u} of size n

• Output:
$$\vec{v} \cdot \vec{u} = \sum_i v_i u_i$$
.



Example 1: Inner product (cont.)

• Input: vectors \vec{v} , \vec{u} of size n

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- 1. Make a *p*-way distribution of \vec{v}, \vec{u} (e.g. in blocks), resulting in subvectors $\vec{v}^{(s)}$ and $\vec{u}^{(s)}$.
- These subvectors are then split into tokens that each fit in L.
 We have two streams for each core s:

$$\Sigma_{\vec{v}}^{s} = ((\sigma_{\vec{v}}^{s})_{1}, (\sigma_{\vec{v}}^{s})_{2}, \dots, (\sigma_{\vec{v}}^{s})_{H}),$$

$$\Sigma_{\vec{u}}^{s} = ((\sigma_{\vec{u}}^{s})_{1}, (\sigma_{\vec{u}}^{s})_{2}, \dots, (\sigma_{\vec{u}}^{s})_{H}).$$

3. Maintain a partial answer α_s throughout the algorithm, add $(\sigma_{\vec{v}}^s)_h \cdot (\sigma_{\vec{u}}^s)_h$ in the *h*th hyperstep. After the final tokens, sum over all α_s .

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- Input: Matrices A, B of size $n \times n$
- Output: C = AB

We decompose the (large) matrix multiplication into smaller problems that can be performed on the accelerator (with $N \times N$ cores). This is done by decomposing the input matrices into $M \times M$ outer blocks, where M is chosen suitably large.

$$AB = \begin{pmatrix} A_{11} & A_{12} & \dots & A_{1M} \\ \hline A_{21} & A_{22} & \dots & A_{2M} \\ \hline \vdots & \vdots & \ddots & \vdots \\ \hline A_{M1} & A_{M2} & \dots & A_{MM} \end{pmatrix} \begin{pmatrix} B_{11} & B_{12} & \dots & B_{1M} \\ \hline B_{21} & B_{22} & \dots & B_{2M} \\ \hline \vdots & \vdots & \ddots & \vdots \\ \hline B_{M1} & B_{M2} & \dots & B_{MM} \end{pmatrix}$$

We compute the **outer blocks** of C in row-major order. Since:



a complete outer block is computed every *M* hypersteps, where in a hyperstep we perform the multiplication of one outer blocks of *A*, and one of *B*.

Each block is again decomposed into **inner blocks** that fit into a core:

$$A_{ij} = \begin{pmatrix} (A_{ij})_{11} & (A_{ij})_{12} & \dots & (A_{ij})_{1N} \\ \hline (A_{ij})_{21} & (A_{ij})_{22} & \dots & (A_{ij})_{2N} \\ \hline \vdots & \vdots & \ddots & \vdots \\ \hline (A_{ij})_{N1} & (A_{ij})_{N2} & \dots & (A_{ij})_{NN} \end{pmatrix}$$

We compute the **outer blocks** of *C* in row-major order. Since:

$$C_{ij} = \sum_{k=1}^{M} A_{ik} B_{kj},$$

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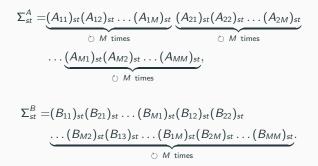
The streams for core (s, t) are the inner blocks of A that belong to the core, laid out in row-major order, and the inner blocks of B in column-major order.



$$\Sigma_{st}^{B} = (B_{11})_{st}(B_{21})_{st} \dots (B_{M1})_{st}(B_{12})_{st}(B_{22})_{st}$$

$$\underbrace{\dots (B_{M2})_{st}(B_{13})_{st} \dots (B_{1M})_{st}(B_{2M})_{st} \dots (B_{MM})_{st}}_{\bigcirc M \text{ times}}.$$

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In a hyperstep a suitable BSP algorithm (e.g. Cannon's algorithm) is used for the matrix multiplication on the accelerator.

We show that the cost function can be written as:

$$\tilde{T}_{\text{cannon}} = \max\left(2\frac{n^3}{N^2} + \frac{2Mn^2}{N}g + NM^3I, \ 2\frac{Mn^2}{N^2}e\right)$$

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- *Input*: An array A of comparable objects.
- Output: The sorted array \tilde{A} .
- Parallel bucket sort: create p buckets, put each element of A in the appropriate bucket, let the sth core sort the sth bucket.
- Sample sort samples elements of A in order to balance the buckets.

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- 2. **Sample sort** samples elements of *A* in order to balance the buckets.

- Split the input array to create p equally sized streams. Also create p initially empty streams that will be the buckets.
- 2. We adapt the sample sort algorithm, first we need to find the buckets, which is **Phase 1** of our algorithm.
- Each core samples k elements randomly from its stream. We do this using a classic streaming algorithm called *reservoir sampling*. These samples are then sorted.

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• In Phase 2 of the algorithm we fill the buckets with data.

- In a hyperstep, we run a BSP sort on the current tokens. Next, each core will have consecutive elements that can be sent to the correct buckets efficiently.
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- Parallella and the Epiphany: great platform for BSP.
- Pseudo-streaming algorithms are a convenient way to think about algorithms for this platform.
- Can often (re)use BSP algorithms, and generalize them to this streaming framework, even if local memory is limited.

Thank you for your attention. Questions?

- Parallella, Adapteva Epiphany: http://www.adapteva.org
- 2. Epiphany BSP: http://www.codu.in/ebsp
- KiloCore: https://www.ucdavis.edu/news/ worlds-first-1000-processor-chip